IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A process comprising:

mating a microelectronic die substrate to a board, wherein the substrate includes an upper surface, a lower surface, and a solder first bump disposed on the lower surface; and while mating

forming a stress-compensation collar (SCC) on the board, wherein the SCC abuts the solder first bump.

2. (Original) The process of claim 1, wherein forming the SCC includes embedding the solder first bump into the SCC to a depth range from about 5 percent embedded to about 95 percent embedded.

3. (Original) The process of claim 1, further including reflowing the solder first bump.

4. (Original) The process of claim 1, further including:

reflowing the solder first bump; and

curing the SCC.

5. (Original) The process of claim 1, wherein forming an SCC includes dispensing an SCC mass on the board.

6. (Original) The process of claim 1, wherein forming an SCC includes dispensing an SCC mass on the board, wherein the SCC mass includes a plurality of spaced-apart spots.

7. (Original) The process of claim 1, wherein mating includes mating through an uncured organic composition that includes a non-fugitive element in the composition, and wherein the composition includes at least one material selected from an epoxy solder paste, an epoxy flux, and combinations thereof.

8. (Original) The process of claim 1, wherein mating includes mating through an uncured organic composition that includes a non-fugitive element in the composition, and wherein the composition includes at least one material selected from a resin-containing flux, a cyanate ester-containing flux, a polyimide-containing flux, a polybenzoxazole-containing flux, a polybenzimidazole-containing flux, a polybenzothiazole-containing flux, a polymer-solder-flux paste, and combinations thereof.

9. (Original) The process of claim 1, wherein mating includes mating through an uncured organic composition that includes a non-fugitive element in the composition, and wherein the composition includes at least one material selected from a paste, a solder paste, an epoxy-containing solder paste, a resin-containing paste, a cyanate ester-containing paste, a polyimide-containing paste, a polybenzoxazole-containing paste, a polybenzimidazole-containing paste, a polybenzothiazole-containing paste, a flux, and combinations thereof.

10. (Original) The process of claim 1, wherein forming an SCC includes dispensing a single SCC mass on the board.

11. (Original) The process of claim 1, before mating, the process including:

forming a stress-relief layer (SRL) upon the substrate lower surface, wherein the SRL partially embeds the solder first bump.

12. (Original) The process of claim 1, further including:

forming an SRL upon the substrate lower surface, wherein the SRL partially embeds the solder first bump; and

reflowing the solder first bump.

13. (Original) The process of claim 1, further including:

forming an SRL upon the substrate lower surface, wherein the SRL partially embeds the solder first bump;

reflowing the solder first bump; and

curing at least one of the SCC and the SRL.

14. (Original) The process of claim 1, further including:

forming an SRL upon the substrate lower surface, wherein the SRL partially embeds the solder first bump, and wherein forming includes dispensing the SRL by ejecting a discrete series of quanta of polymer masses upon the lower surface that includes a ball grid array in excess of four solder bumps including the solder first bump.

Claims 15 - 29. (Canceled)

30. (Currently amended) A process comprising:

forming a stress-relief layer peripheral ring on a microelectronic die substrate that touches a plurality of peripheral solder bumps on the microelectronic die substrate;

mating [[a]] the microelectronic die substrate to a board, wherein the microelectronic die substrate includes an upper surface, a lower surface, and [[a]] the plurality of peripheral solder bumps ~~first bump~~ disposed on the lower surface; and while mating

forming a stress-compensation collar (SCC) on the microelectronic die substrate ~~board~~, wherein the SCC abuts the plurality of peripheral solder bumps ~~first bump~~, and wherein forming the SCC includes ~~dispensing~~ a stream of mass disposed upon the microelectronic die substrate ~~board~~ and under conditions to embed the plurality of peripheral solder bumps ~~first bump~~.

31. (Currently amended) The process of claim 30, wherein forming a stress-compensation collar ~~dispensing~~ includes embedding the plurality of peripheral solder bumps ~~first bump~~ into the SCC to a depth range from about 5 percent embedded to about 95 percent embedded.

32. (Currently amended) The process of claim 30, wherein forming a stress-compensation collar ~~dispensing~~ includes using an X-Y gantry to deposit the SCC.

33. (Currently amended) The process of claim 30, wherein forming a stress-compensation collar ~~dispensing~~ includes using an X-Y gantry to deposit the SCC, and wherein the stream of mass substantially contacts about half or more of each ~~the~~ circumference of the plurality of peripheral solder bumps ~~first bump~~.

34. (Currently amended) The process of claim 30, wherein forming a stress-compensation collar ~~dispensing~~ includes using an X-Y gantry to deposit the SCC, and wherein the stream of mass substantially contacts about half or more of the circumference of each ~~the~~ circumference of the plurality of peripheral solder bumps ~~first bump~~, and wherein forming a stress-compensation collar ~~dispensing~~ includes embedding the plurality of peripheral solder bumps ~~first bump~~ into the SCC to a depth range from about 5 percent embedded to about 95 percent embedded.

35-39. (Canceled)

40. (Currently amended) A process comprising:

forming a stress-relief layer peripheral ring on a microelectronic die substrate that touches a plurality of peripheral solder bumps on the microelectronic die substrate;

mating [[a]] the microelectronic die substrate to a board, wherein the microelectronic die substrate includes an upper surface, a lower surface, and [[a]] the plurality of peripheral solder bumps ~~first bump~~ disposed on the lower surface; and while mating

forming a stress-relief layer on the microelectronic die substrate ~~board~~, wherein the stress-relief layer abuts the plurality of peripheral solder bumps ~~first bump~~, and wherein forming the stress-relief layer includes dispensing a discrete series of a polymer mass upon the microelectronic die substrate ~~board~~ and under conditions to embed the plurality of peripheral solder bumps ~~first bump~~.

41. (Currently amended) The process of claim 40, wherein forming a stress-relief layer on the microelectronic die substrate ~~board~~ dispensing includes embedding the plurality of peripheral solder bumps ~~first bump~~ into the stress-relief layer to a depth range from about 5 percent embedded to about 95 percent embedded.

42. (Previously Presented) The process of claim 40, wherein dispensing includes using an X-Y gantry to deposit the stress-relief layer.

43. (Canceled).